**Inverters**

\begin{picture}
% latex2html id marker 337
(15,10)
%
% outline of 14 pin chip
%
...
 ...{3}{\line(3,-5){0.9}}
\multiput(4.4,8.0)(4,0){3}{\line(-3,-5){0.9}}\end{picture}

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| LS04 | : | Hex inverters. |  | 9.5ns |

**Two Input Gates**

\begin{picture}
% latex2html id marker 412
(15,10)
%
% outline of 14 pin chip
%
...
 ...,0){2}{\circle{0.35}}
\multiput(7.5,6.5)(6,0){2}{\oval(1.6,3.0)[t]}\end{picture}

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| LS00 | : | Quad 2-input nand gates. |  | 9.5ns |
| LS08 | : | Quad 2-input and gates. |  | 9.0ns |
| LS32 | : | Quad 2-input or gates. |  | 14ns |
| LS86 | : | Quad exclusive or gates. |  | 10ns |

**Two Input Nor Gates**

\begin{picture}
% latex2html id marker 495
(15,10)
%
% outline of 14 pin chip
%
...
 ...,0){2}{\circle{0.35}}
\multiput(3.5,6.5)(6,0){2}{\oval(1.6,3.0)[t]}\end{picture}

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| LS02 | : | Quad 2-input nor gates. |  | 10ns |

**Three Input Gates**

\begin{picture}
% latex2html id marker 578
(15,10)
%
% outline of 14 pin chip
%
...
 ...,0){2}{\circle{0.35}}
\multiput(5.5,6.5)(8,0){2}{\oval(1.6,3.0)[t]}\end{picture}

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| LS10 | : | Triple 3-input nand gates. |  | 9.5ns |
| LS11 | : | Triple 3-input and gates. |  | 9.0ns |
| LS27 | : | Triple 3-input nor gates. |  | 10ns |

**Four Input Gates**

\begin{picture}
% latex2html id marker 660
(15,10)
%
% outline of 14 pin chip
%
...
 ...6}}
\put(11.5,1.8){\circle{0.35}}
\put(11.5,3.5){\oval(1.6,3.0)[b]}\end{picture}

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| LS20 | : | Dual 4-input nand gates. |  | 9.5ns |
| LS21 | : | Dual 4-input and gates. |  | 9.0ns |

**Eight Input Nand Gates**

\begin{picture}
% latex2html id marker 735
(15,10)
%
% outline of 14 pin chip
%
...
 ...}}
%
\put(7.5,9.0){\line(0,-1){2.6}}
\put(7.5,6.4){\line(1,0){3.5}}\end{picture}

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| LS30 | : | Single 8-input nand gates. |  | 10.5ns |

**Thirteen Input Nand Gates**

\begin{picture}
% latex2html id marker 801
(17,10)
%
% outline of 16 pin chip
%
...
 ...
\put(12.5,8.3){\line(0,-1){0.9}}
\put(12.5,7.4){\line(1,0){0.5}}
%\end{picture}

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S133 | : | Single 13-input nand gates. |  | 6ns |

**Octuple Bus Drivers**

\begin{picture}
% latex2html id marker 1681
(21,10)
%
% outline of 20 pin chip
%...
 ...s
\put(3.5,9.0){\line(0,-1){3.2}}
\put(3.5,5.8){\line(1,0){14.7}}
%\end{picture}

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| LS240 | : | Octal inverting three-state buffers. |  | 10.5ns |
| LS244 | : | Octal non-inverting three-state buffers. |  | 12ns |

**Synchronous 4-bit Binary Counters**

\begin{picture}
% latex2html id marker 2241
(17,10)
%
% outline of 16 pin chip
%...
 ...6.5){\makebox(0,0){outputs}}
\put(7.5,4.5){\makebox(0,0){inputs}}
%\end{picture}

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| LS161A | : | Synchronous 4-bit binary counter. |  | 14ns |

The LS161A binary counter has a positive edge triggered clock input CLK, and a negative logic asynchronous clear input $\overline{\rm CLR}$.The value stored in the counter is continuously presented on the Q outputs (${\rm Q}_0$ is least significant, positive logic is used).

When $\overline{\rm LD}$is held low, data from the D inputs will be loaded into the counter when it is clocked. When ${\rm EN}_T$, ${\rm EN}_P$and $\overline{\rm LD}$are all held high, the counter will increment when clocked. Holding either ${\rm EN}_T$or ${\rm EN}_P$inputs low will inhibit counting. The ${{\rm C}_{out}}$output indicates that the counter holds the value 1111 and the ${\rm EN}_T$input is high.

To build high precision synchronous counters, wire the ${{\rm C}_{out}}$output of each stage to the ${\rm EN}_T$input of the next more significant stage, and wire the CLK, $\overline{\rm CLR}$, $\overline{\rm LD}$and ${\rm EN}_P$inputs in parallel across all stages.